

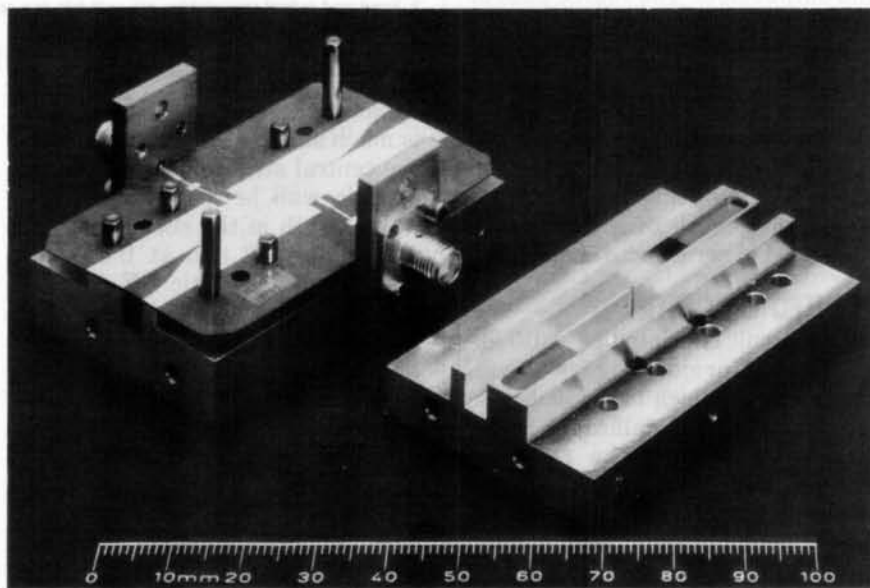
COPLANAR BIAS STABILIZES GAIN IN FINLINE AMPS

DC inputs provide low-VSWR impedance to prevent oscillations at frequencies below cutoff.

FINLINES enable microwave amplifiers to operate efficiently at frequencies at which other transmission lines become lossy or difficult to fabricate. At frequencies below cutoff, however, finlines become reactive and tend to cause unwanted oscillations. Fortunately, low-frequency transmission lines can be used in the bias networks to provide stability without compromising performance.

Unconditionally stable amplification is difficult to achieve in finline environments. Impedance matching and the suppression of undesirable feedback are more difficult in finline than in other transmission structures such as microstrip. Additionally, at frequencies below cutoff, finline becomes reactive with high

JEAN L'ECUYER, Spar Aerospace Ltd., Ste-Anne-de-Bellevue, Quebec, Canada; WOLFGANG J.R. HOEFER, University of Ottawa, Department of Electrical Engineering, Ottawa, Ontario, Canada; and GREGORY B. GAJDA, Millennium Microwave Corp., Ottawa, Ontario, Canada; (613) 596-6728



1. A 17-GHz finline amplifier uses parallel finlines separated by a thin metallic wall or septum. Microstrip lines provide DC bias and stable impedances below the finline cutoff frequency. (Photo courtesy of the Dept. of Communications, Canada.)

VSWR, increasing the potential for oscillations at lower frequencies.

To overcome these difficulties, some designs place the FET in a microstrip mount with antipodal finline transitions to the input and output waveguide ports. To stabilize the device at frequencies below cutoff, dissipative slots are added to each transition. Although good RF-to-DC isolation can be achieved with this technique, the absorbing material and long, lossy transitions degrade the amplifier's performance, particularly when it is integrated

into a finline subassembly.

By modifying a configuration proposed by Jacob and Ansorge,¹ an unconditionally stable finline amplifier can be realized (Fig. 1). Rather than placing input and output finlines at right angles, the modified amplifier uses parallel finlines. Shielded from each other by a thin metallic wall or septum, both of the unilateral, single-fin lines exhibit half the impedance of symmetrical finlines. The transistor is mounted in a narrow opening of the septum (Fig. 2), and

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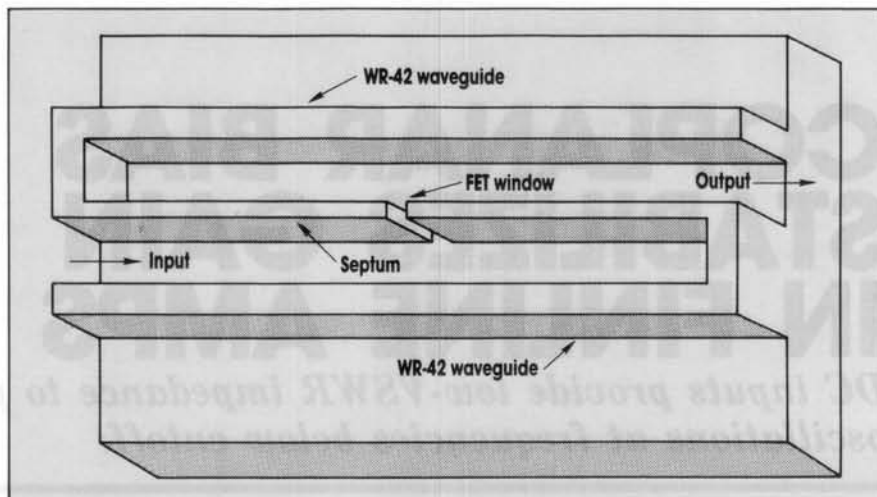
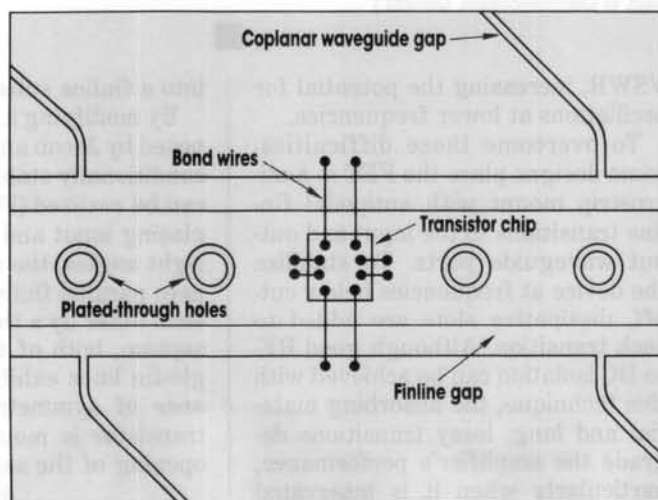
is coupled magnetically to the input and output lines with bond wires (Fig. 3).

In the prototype amplifier, both ports originate with WR-42 waveguide and are tapered to single-fin, unilateral lines with a gap width of 0.18 mm (Fig. 4). The single-fin lines have a power-voltage impedance of $83\ \Omega$ and an effective dielectric constant of 1.11 at 16.8 GHz. Bond wires attached to the gate and drain pads of the transistor are bonded to the metallization across the input and output slots. The source pads of the FET chip are grounded to the central metallization. For maximum magnetic coupling, the finlines are short-circuited about one-quarter wavelength beyond the bond wires. Input and output ports are matched to the FET by using silver paint to adjust the length of a tuning slot connected in series with each line.

PRINTED CIRCUITRY

The circuit is printed on 0.010-in.-thick RT/Duroid (Rogers Corp., Rogers, CT), which has a dielectric constant of 2.22. Metallization is unilateral except for the serrated clamping regions, the microstrip sections, and the central strip. A series of plated-through holes extend the septum through the dielectric. The holes have 0.35-mm diameter, and their centers are 1 mm apart.

3. The FET is mounted on the center strip that bridges the septum through the dielectric substrate. Bond wires provide magnetic coupling to the finlines.



2. Input and output waveguides are split into two sections. The printed circuit is mounted between sections to form single-fin lines.

Because the spacing between holes is much smaller than a wavelength, the central strip forms an effective electric wall between waveguides (wavelength in the substrate is approximately 12 mm at the design frequency). Parasitic RF coupling between input and output ports is less than -30 dB from 15 to 20 GHz (Fig. 5).

The transistor chip, an NEC NE67300 (California Eastern Laboratories, Santa Clara, CA), was selected for its low noise performance at the frequency of interest. A standard transistor model was used in the design and analysis of the amplifier. The characteristics of the model were based on S-parameters pro-

vided by the manufacturer for frequencies between 2 and 18 GHz and $50\text{-}\Omega$ characteristic impedance. The inductance of each pair of bond wires that couple the transistor terminals to the slots was estimated to be 0.5 nH.

Maximum available gain of the NE67300 is about 10 dB at 17 GHz. However, corresponding input and output impedances are very close to unstable regions on a Smith chart. To improve stability, the amplifier was designed for only 9-dB gain. The selected source and load impedances are $10 + j16$ and $31 + j46\ \Omega$, respectively. These impedances are situated well within stable regions on a Smith chart.

Input- and output-matching networks contain adjustable elements in the form of short-circuited stubs connected at appropriate distances from the FET.² Again, fine tuning was achieved by adjusting the length of the stubs with silver paint.

STABILIZING BIAS

Special gate and drain bias circuits were developed to overcome the problem of amplifier instability at frequencies below the finline cut-off frequency (6 GHz) without degrading amplifier performance. To achieve this goal, bias circuits must be electrically invisible to the tran-

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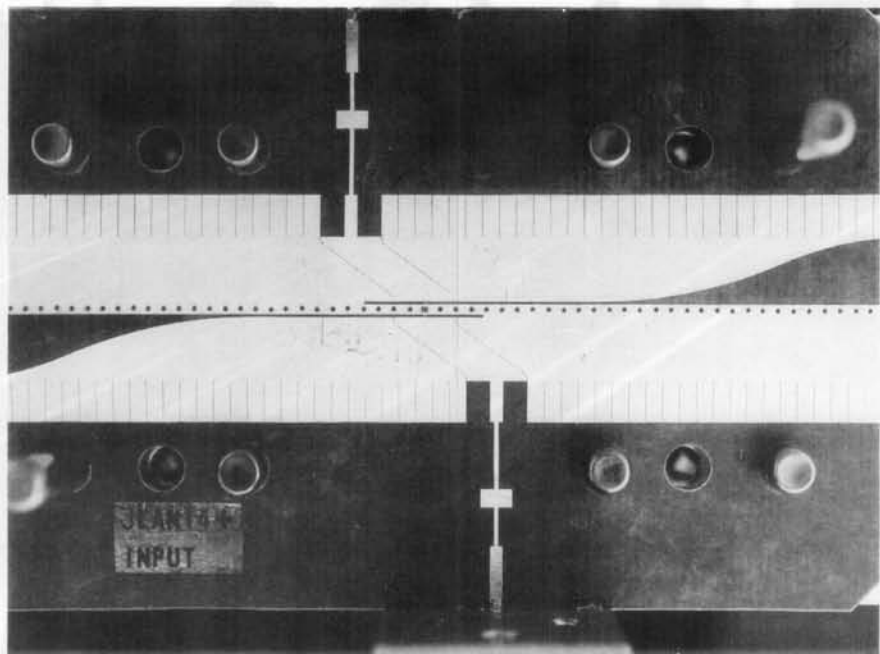
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4. Half-wavelength coplanar lines extend from the waveguide wall to the FET. Finlines are terminated one-quarter wavelength from the FET with tuning stubs connected in series. (Photo courtesy of the Dept. of Communications, Canada.)

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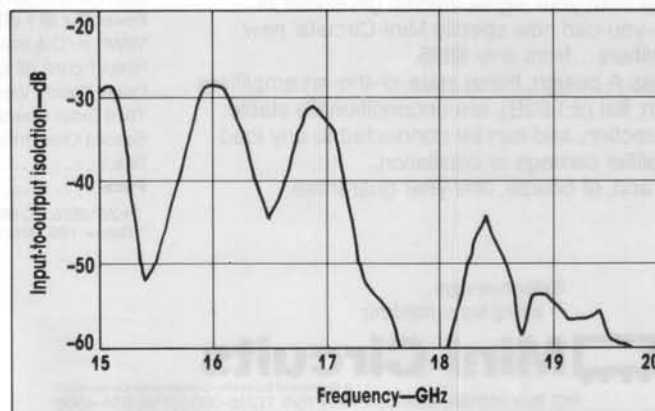
sistor at RF while presenting stable loads at lower frequencies where the finlines become reactive and produce high VSWR.

The bias circuits use coplanar waveguide formed by two narrow parallel slots in the fins. At the amplifier's center frequency (16.8 GHz), the coplanar sections measure one-half wavelength between the bond wires and the waveguide's outer wall. The half-wavelength lines transform the RF short circuit at the waveguide wall into an RF

short circuit at the finline edge. The length of the coplanar sections (7.11 mm) could only be accommodated in WR-42 waveguide by running the sections at an angle of about 45 deg.

At the outer broad wall, the coplanar section is transformed into a microstrip line that is terminated with a 50-Ω load through a bias tee. A microstrip low-pass filter reduces RF leakage into the bias circuit. Leakage at the amplifier's operating frequency is approximately -27 dB (Fig. 6). Because the bias circuit is composed of microstrip and coplanar waveguide, stable 50-Ω imped-

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5. Measured with the transistor removed, input-to-output isolation is better than 30 dB at 17 GHz. The close spacing of plated-through holes provides effective electric shielding.

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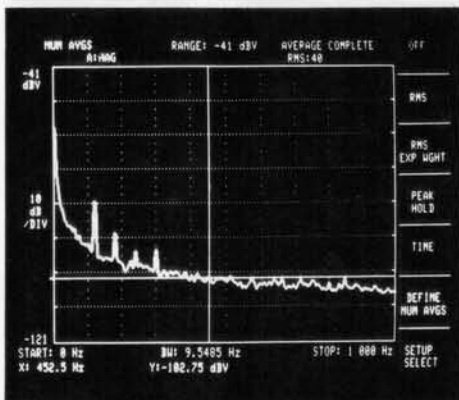
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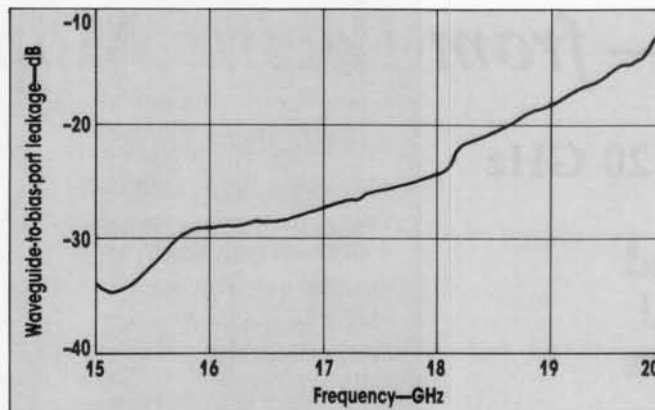
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6. Waveguide-to-bias-port leakage was measured with the bias ports terminated by 50- Ω impedances. Leakage was reduced using low-pass microstrip filters.

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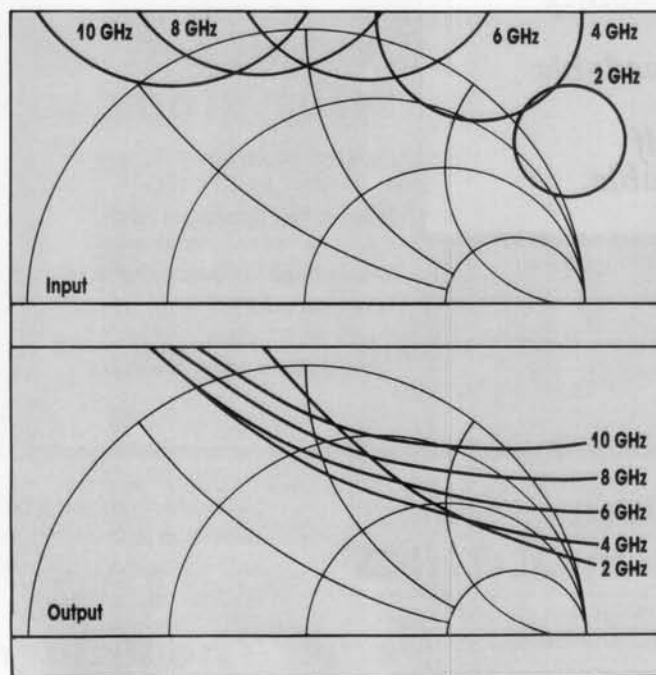
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ances are easily presented to the FET from DC to the cutoff frequency of the microstrip filter. Beyond the filter's cutoff frequency, stable impedances are presented by the finlines.

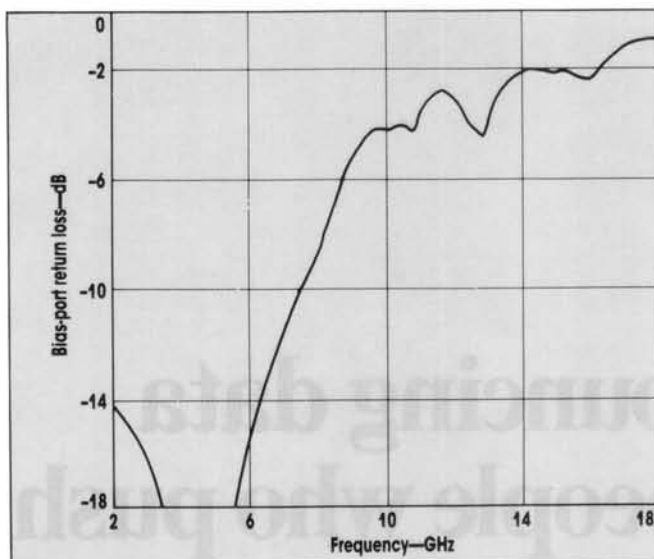
To guarantee unconditional stability, it is important to consider all potentially unstable operating conditions. For the NE67300 FET, the most unstable frequencies are between 4 and 5 GHz (Fig. 7). To prevent the transistor from oscillating, the bias circuit was designed for minimum VSWR in this frequency range.

The performance of the bias circuits was verified by replacing the transistor with a 50- Ω chip resistor and measuring the reflection coefficient at the bias input ports. Return loss was better than the minimum required for all frequencies. From 3.5 to 5.6 GHz, S_{11} was less than -18 dB (Fig. 8).

Tuning was performed while measuring the amplifier response in a network analyzer. The tuning stubs were accessible through an opening in the sidewall of the housing that is situated above the transistor. Once the amplifier was tuned, the opening was closed with a brass cover. Since most of the electromagnetic energy is concentrated in and



7. Input and output stability circles indicate that the transistor is most likely to oscillate at frequencies between 4 and 5 GHz. The bias circuit was designed to present minimum VSWR to the transistor at these frequencies.



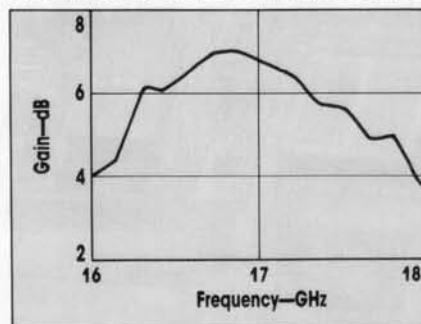
8. Return loss at the bias ports was measured by replacing the FET with a 50- Ω chip resistor. The circuit provides low VSWR below the finline cutoff frequency of 6 GHz.

around the finline slot, the sidewall opening has no significant effect on the circuit's response.

AMPLIFIER PERFORMANCE

Before tuning, the circuit had only about 4-dB gain at the design frequency. This was probably due to the fact that the influence of the plated-through holes on finline impedance had been ignored. After tuning, the amplifier was unconditionally stable at all frequencies, and gain was better than 6 dB over a 1-GHz bandwidth centered at 16.8 GHz (Fig. 9). Noise figure was 3.5 dB at that frequency.

Failure to achieve 9-dB gain is probably due to several factors that were not considered during the design. Losses in the input and output networks, tolerances in device pa-



9. The finline amplifier achieves 7-dB gain with 3.5-dB noise figure and demonstrates an effective method of directly embedding active devices in a finline environment.

rameters, and differences in the circuit environment could reduce the amplifier's gain. Additionally, the 50- Ω S-parameters that were used in the design were not measured using a finline mount. The electromagnetic fields in finline would probably have produced slightly different values.

However, the techniques of magnetically coupling the transistor to the finlines and biasing the device through coplanar waveguide were successful. The amplifier's performance encourages the design of other finline components, such as oscillators, mixers, and frequency multipliers, using these techniques.

Although microwave oscillators can be realized by mounting FETs in finline, spurious oscillations are often a problem. The use of coplanar bias in finline oscillators should enable greater control over oscillation conditions. ••

Note

The work discussed in this article was performed at the Dept. of Communications, Communications Research Center, Ottawa, Ontario, Canada.

Acknowledgment

The authors gratefully acknowledge the valuable assistance given by the staff of the Communications Research Center, Ottawa, Ontario, Canada. In particular, the many helpful suggestions by C. Verver, B. Clarke, and R. Douville concerning the stability of FETs in E-plane and finline structures were highly appreciated.

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